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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,382	11/26/2003	Hien Boon Tan	Q78432	6007

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/721,382	TAN ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1page*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 15-20 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12-20-5.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 7 and 10-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 5, 7 and 14, the language "one of a group comprising" is improper Markush language.

In claim 10 there is insufficient antecedent basis for the language "said section face."

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for

purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5-8, 10, 11 and 14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Foster (6552416).

In the abstract, and at column 1, line 42 to column 2, line 7; column 2, lines 26-38; column 3, line 18 to column 4, line 16; column 4, lines 42-49; and column 4, line 67 to column 5, line 3, Foster discloses the following:

An integrated circuit package, comprising: a) a die pad 14 having a first face and a second face opposite to said first face; b) a plurality of inner leads 20 each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of inner leads is disposed substantially co-planar with and substantially around said die pad; c) a plurality of outer leads 12 each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of outer leads is disposed substantially co-planar with and substantially around said plurality of inner leads and said die pad, such that said sides of each of said plurality of outer leads are substantially offset from said sides of each of said plurality of inner leads; d) a first adhesive layer 33 disposed on said first face of said die pad; e) a second adhesive layer 33 disposed on said first face of said plurality of inner leads; f) an integrated circuit chip 31 having a first face and a second face opposite to said first

face, wherein said second face of said integrated circuit chip is coupled to said first face of said die pad through said first adhesive layer, and wherein said second face of said integrated circuit chip is further coupled to said first face of said plurality of inner leads through said second adhesive layer; g) a first plurality of wires 35 linking said plurality of inner leads to said integrated circuit chip, each of said first plurality of wires comprising: a first end electrically conductively joined to said first face of one of said plurality of inner leads, and a second end electrically conductively joined to said first face of said integrated circuit chip; and h) a second plurality of wires 35 linking said plurality of outer leads to said integrated circuit chip, each of said second plurality of wires comprising: a first end electrically conductively joined to said first face of one of said plurality of outer leads, and a second end electrically conductively joined to said first face of said integrated circuit chip; i) an encapsulant 37 surrounding at least said first face of said die pad, said first faces of said plurality of inner leads, said first faces of said plurality of outer leads, said first adhesive layer, said second adhesive layer, said first plurality of wires, said second plurality of wires, and said integrated circuit chip; wherein said first plurality of wires and said second plurality of wires are composed of one of a group comprising: "gold," gold with some level of impurities, aluminum, and copper; a conductive element 30 having a first face and a second face opposite to said first face, wherein said conductive

element is sandwiched between said die pad and said integrated circuit chip, such that said second face of said conductive element is coupled to said first face of said die pad through said first adhesive layer; said second face of said conductive element is further coupled to said first faces of said plurality of inner leads through said second adhesive layer, and said first face of said conductive element is coupled to said second face of said integrated circuit chip through a third adhesive layer 33; j) at least one first linking wire 35 linking said integrated circuit chip to said conductive element, said at least one first linking wire having a first end electrically conductively joined to said first face of said conductive element, and a second end electrically conductively joined to said first face of said integrated circuit chip; and k) at least one second linking wire linking said die pad to said conductive element, said at least one second linking wire having a first end electrically conductively joined to said first face of said conductive element, and a second end electrically conductively joined to said first face of said die pad; wherein said second plurality of wires, said at least one first linking wire and said at least one second linking wire are composed of one of a group comprising: "gold," gold with some level of impurities, aluminum, and copper; and l) an encapsulant surrounding at least said first face of said die pad, said first faces of said plurality of inner leads, said first faces of said plurality of outer leads, said first adhesive, said second adhesive, said

conductive element, said third adhesive, said IC chip, said first plurality of wires, said second plurality of wires, said first linking wire, and said second linking wire.

An integrated circuit package, comprising: a) a die pad having a first face and a second face opposite to said first face; b) a plurality of inner leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of inner leads is disposed substantially co-planar with and substantially around said die pad; c) a plurality of outer leads each having a first face and a second face opposite to said first face, and a plurality of sides between said first face and said second face, wherein said plurality of outer leads is disposed substantially co-planar with and substantially around said plurality of inner leads and said die pad, such that said sides of each of said plurality of outer leads are substantially offset from said sides of each of said plurality of inner leads; d) a first adhesive layer disposed on said first face of said die pad; e) a second adhesive layer disposed on said first face of said plurality of inner leads; f) a first integrated circuit chip 30 having a first face and a second face opposite to said first face, wherein said section face of said first integrated circuit chip is coupled to said first face of said die pad through said first adhesive layer, and wherein said second face of said first integrated circuit chip is further coupled to said first face of said plurality of

inner leads through said second adhesive layer; g) a third adhesive layer disposed on said first face of said first integrated circuit chip; h) a second integrated circuit chip 31 having a first face and a second face opposite to said first face, wherein said second face of said second integrated circuit chip is coupled to said first face of said first integrated circuit chip through said third adhesive layer; i) a first plurality of wires 35 linking said plurality of inner leads to said first integrated circuit chip, each of said first plurality of wires comprising: a first end electrically conductively joined to said first face of one of said plurality of inner leads, and a second end electrically conductively joined to said first face of said first integrated circuit chip; and a second plurality of wires 35 linking said plurality of outer leads to said second integrated circuit chip, each of said second plurality of wires comprising: a first end electrically conductively joined to said first face of one of said plurality of outer leads, and a second end electrically conductively joined to said first face of said second integrated circuit chip; k) an encapsulant surrounding at least said first face of said die pad, said first faces of said plurality of inner leads, said first faces of said plurality of outer leads, said first adhesive layer, said second adhesive layer, said first integrated circuit chip, said third adhesive layer, said second integrated circuit chip, said first plurality of wires, and said second plurality of wires;

wherein said plurality of wires is composed of one of a group comprising: "gold," gold with some level of impurities, aluminum, and copper.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3, 4, 9, 12 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Foster as applied to claims 1, 2, 8, 10 and 11, and further in combination with Kinsman (20040021229).

Foster does not appear to explicitly disclose wherein said encapsulant is a polymer-based molding compound; and wherein said die pad, said

plurality of inner leads, and said plurality of outer leads are composed of a common copper alloy.

Nevertheless, at paragraphs 32 and 36, Kinsman discloses wherein an encapsulant 40 is a polymer-based molding compound; and wherein a die pad 14, a plurality of inner leads 16, and a plurality of outer leads 16 are composed of a common copper alloy. Moreover, it would have been obvious to combine this disclosure of Kinsman with the disclosure of Foster because it would facilitate provision of the encapsulant, pad and leads of Foster.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
28-Feb-06